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A 600GHz Planar Frequency Multiplier Feed On a Silicon Parabola

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Abstract

A novel quasi-optical all-planar **schottkey** diode frequency doubler has been fabricated and **successfully** produced 1.4mW of output power at **600GHz**. The frequency multiplier circuit utilizes a quad-bridge-diode configuration to obtain inherent isolation between the input and the output circuits without the use of complicated filter structures, Two pairs of polarization switched double-slot antennas are **connected** to the diodes for input and output coupling to free space and substitute for the power dividers commonly required in balanced circuits, Compact coplanar transmission line matching circuits, placed between the antennas and the diodes, are designed to provide an optimum matching only at one frequency each for the maximum conversion **efficiency**. The quad-bridge-diode / antenna circuit **can** then be mounted on a dielectric-filled parabola for coupling to quasi-optical propagation systems without suffering from losses due to substrate modes in GaAs.

A 600 GHz frequency doubler was monolithically fabricated on a 5-roil thick GaAs substrate. The circuit contains four diodes with the same anode size of 1x4 μm^2 on three separate 13x13 μm^2 mesa squares with 0.22 pm-thick n-layer doping profile of $2.6x10^{17}/cm^2$ and the 1 pm-thick buried layer of $5x10^{18}/cm^2$. All four **varactor** diodes fit into a compact 30x30 μm^2 area, Four slot antennas surrounding the diodes are 240 pm-long and 140 pm-apart for the input frequency and 120 pm-long and 70 pm-apart for the output frequency. The antenna slot-widths were 10 urn and 5 urn for the input and output respectively. the complete doubler circuitry exists on one side of the 600 x 600 μm^2 chip which was placed at the focal point of a silicon parabola with 2 cm in **diamter** and 5 mm in focal length.

Two different types of matching circuits were designed and tested. Measurements on one circuit (shunt capacitor matching with 0.12 pm-thick **SiN** dielectric layer) showed the peak frequency conversion of 16 **dB** at 298 GHz and the maximum output power of **1.4mW** at 306 GHz. The second matching cercuit (spiral matching) showed slightly larger conversion loss but broader frequency bandwidth with output power peaks at about 1 GHz interval in the measured frequency bandwidth of 594 to 614 GHz limited by high input pump power. Currently, we are making an effort to eliminated resonances in the measurement **system,** and improve conversion **efficiency** by adding matching layers for the air/silicon parabola interface.

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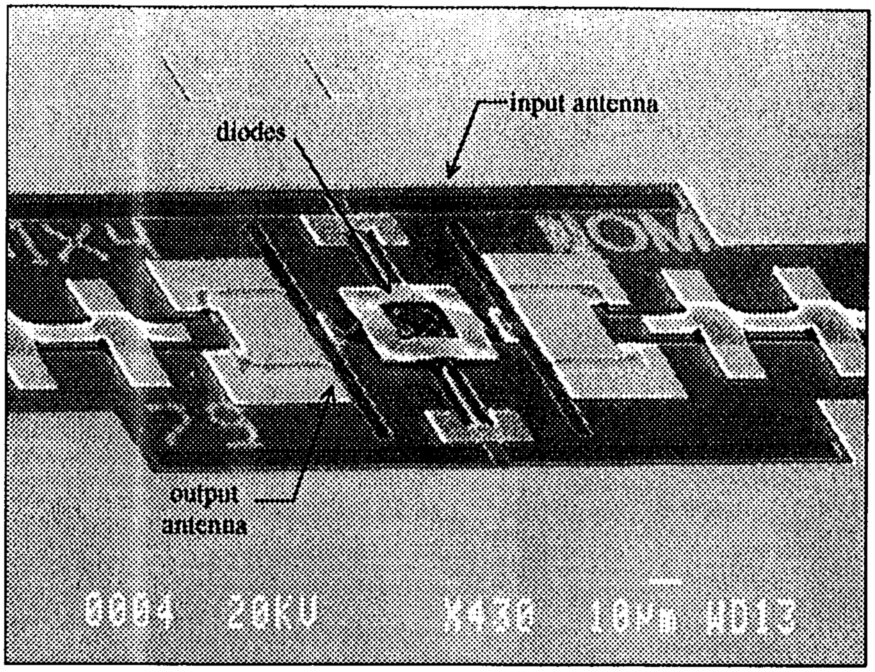

Figure 1. SEM Picture of the quasi-optical frequency doubler. The **dc** bias networks extending to both left and right from the output slot antennas allows us to estimate the RF input power coupling by monitoring the changes on the diodes' dc bias.

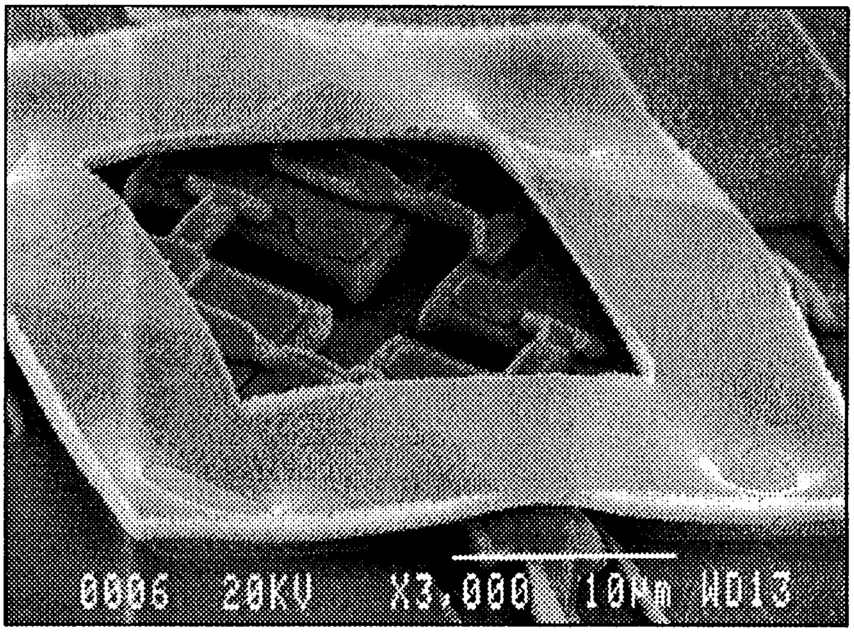

Figure 2. Enlarged view of the quad-diodes in the frequency doubler circuit. The air-bridges, placed 3 **μm** above the four diodes **and** connecting all the ground planes together, suppress slot-line modes on the coplanar transmission lines.

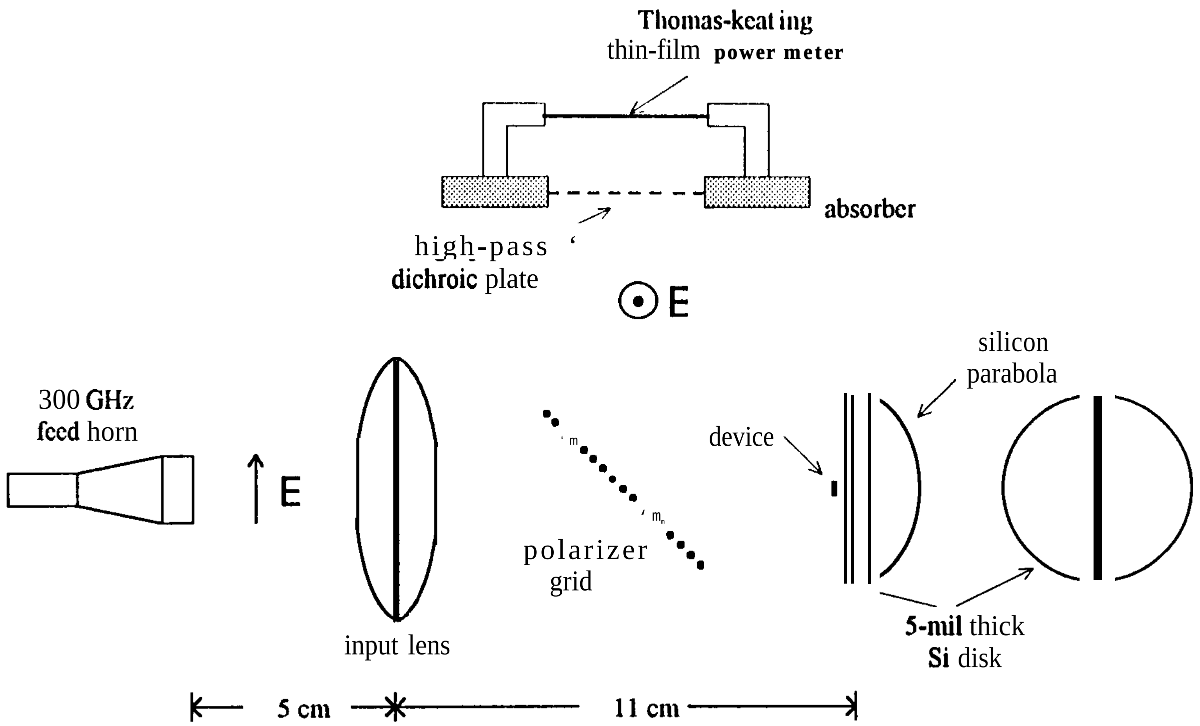

Figure 3. **Mesaurement** setup for the 600GHz doubler. The input lens was designed to produce **7mm beamwaist Gaussian** beam at the **parabola** from 1.25mm feed horn **beamwaist.** In order to **calculate** the conversion loss, the parabola was later replaced with **Thomas-Keating** power meter without the **dichroic** plate to estimate the input power incident onto the parabola.

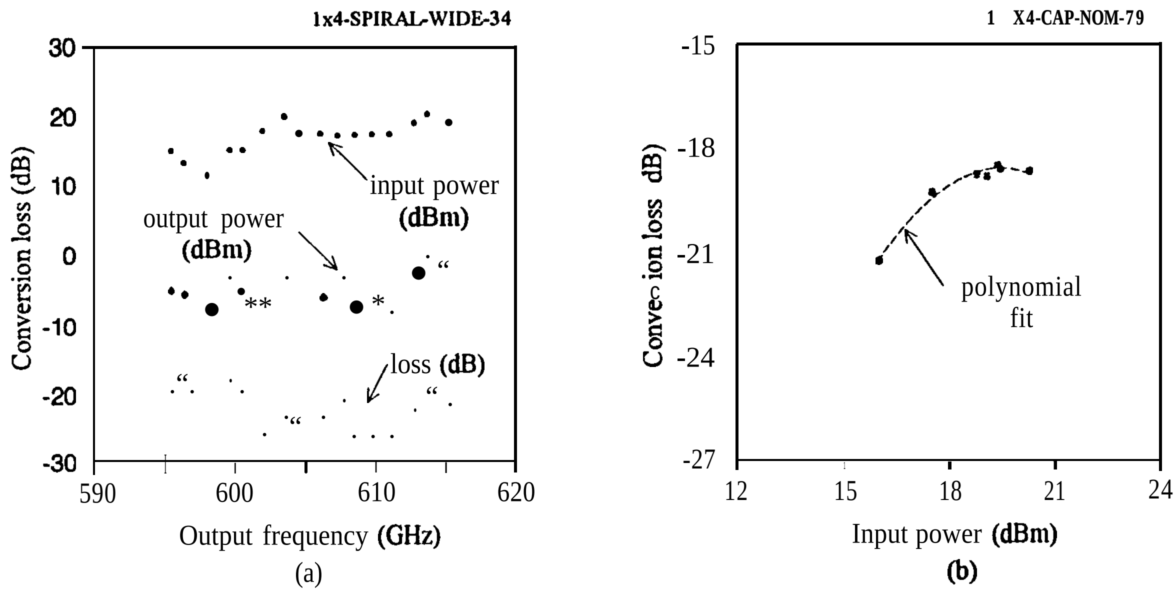

Figure **4**. Measured data, (a) Conversion loss **vs**. output frequency, and **(b)** Conversion loss vs. input power level at the output frequency of614GHz, Input power was available only in the frequency range shown above.